EMB-2239

Technical Specification Manual

Version: R1.00

Revisions

Version	Description of Version	Date Completed
R1.00	Release	08/01/2022

Preface

This Technical Specification Manual (TSM) specifies the board layout, components, connectors, and the I/O connection ports, motherboards features.

Intended Audience

The TSM is intended to provide detailed, technical information about the EMB-2239 and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically not intended for general audiences.

What This Document Contains

Chapter	Description
1	Introduction
2	Product Description
3	Technical Reference
4	Operating System

1. Introduction

1.1 Product introduction

The EMB-2239 embedded board is based on the NXP i.MX8M Plus ARM application processor. The board features a Power over Ethernet (PoE) ready Gigabit Ethernet port, on-board dual-core DSP that runs algorithms for voice control, a full set of I/Os including RS-232/485/CAN, dual MIPI CSI camera interfaces and expansion header slot for PCIe, GPIO and second ethernet port, integrated AI/ML Neural Processing Unit.

1.2 Form Factor

The EMB-2239 is based on Pico-ITX .It is a small Single Board Computer Form factor with 100 x 72 mm (3.9” x 2,8”).

2. Product Description

2.1 Specification

Table 1 summarizes the major features of the board.

Table 1. Specification

Platform	NXP i.MX8M Plus
Form Factor	Pico-ITX
Processor	i.MX 8M Plus Quad
Core	4x ARM Cortex-A53 @ 1.8GHz 1x Arm Cortex-M7 @ 800MHz
System Memory	LPDDR4 @3200MT up to 4GB
Ethernet	1 x GbE with POE option, second RGMII via pin header
Wireless	1x WiFi/Bluetooth (AP6255/56) module, 802.11 b/g/n/ac + Bluetooth v5.0
Audio	1 x mono Class D speaker out @2W(4Ω), 2 (R/L) x HP out header, amplified speaker out (R/L) @ 3W(4Ω) 1x 24-pin FPC expansion header: 8 channel digital audio input and 8 channel digital audio output (SAI1) interfaces with 32-bit @ 384 kHz fs and TDM support
Voice Control Frontend	Dual digital MEMS microphone header via CS47L24 with dual DSP, support multi-mic noise suppression, acoustic echo cancellation (AEC), omni-directional spatial 8 channel digital audio/DMIC inputs (SAI5) via 40-pin expansion header
Storage	Onboard iNAND flash (16GB default), 1x micro SD slot, 265K EEPROM with write protect control
Graphic Controller	GC7000UL supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan
Display Interface	1x micro HDMI, HDMI 2.0a supports 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30
LCD Interface	1x MIPI 4-lane DSI, 1x Dual Channel LVDS for 5”, 7”, 8”, 10.1” and other size LCD panels
Display Resolution	LVDS- up to 1920x1200p60, MIPI DSI - up to 1920x1200p60 or 2x 1080p60 + 1x 4kp30 on HDMI
Camera Interface	2x MIPI-CSI, one camera up to 12MP@30fps / 4kp45 or two up to 1080p80, 2x ISP supporting 375 Mpixel/s
AI/ML	Dedicated Neural Processing Unit (NPU): 2.3 TOPS; PCIe or USB expansion via pin headers
SD Card Socket	1 x micro SD Socket (not support hot plug)
USB	2x USB2.0 or 1x USB3.0 Type A, 2x USB2.0 header
Boot Switch	1 x 2-bit DIP switch for iNAND and micro SD boot selection 1 x bootload button for USB and board boot
Power Switch	1 x on-board power switch
I/O Terminal Block	5-pin header with two combination of RS-232, RS-485 or CAN and 2 x GPIO
RTC	1 x RTC input, 2-pin wafe heder,1.25mm
Power Input	1 x 5VDC power input via header or POE with optional module
OTG	1 x USB 3.0 Type C OTG

Expansion	1x 40-pin connector with PCIe x1, GPIO, font panel control, POE power input and 8 channel audio inputs
Operating Temperature	0 ~ 60°C (32 ~ 140°F)
Storage Temperature	-40 ~ 85° C (-40 ~ 185° F)
Operating Humidity	5% ~ 95%, 40ºC, non-condensing
Dimensions	100 x 72 mm (3.94" x 2.84")

2.2 Board Layout

Figure 1 shows the location of the major components on the top and bottom-side of the EMB-2238.

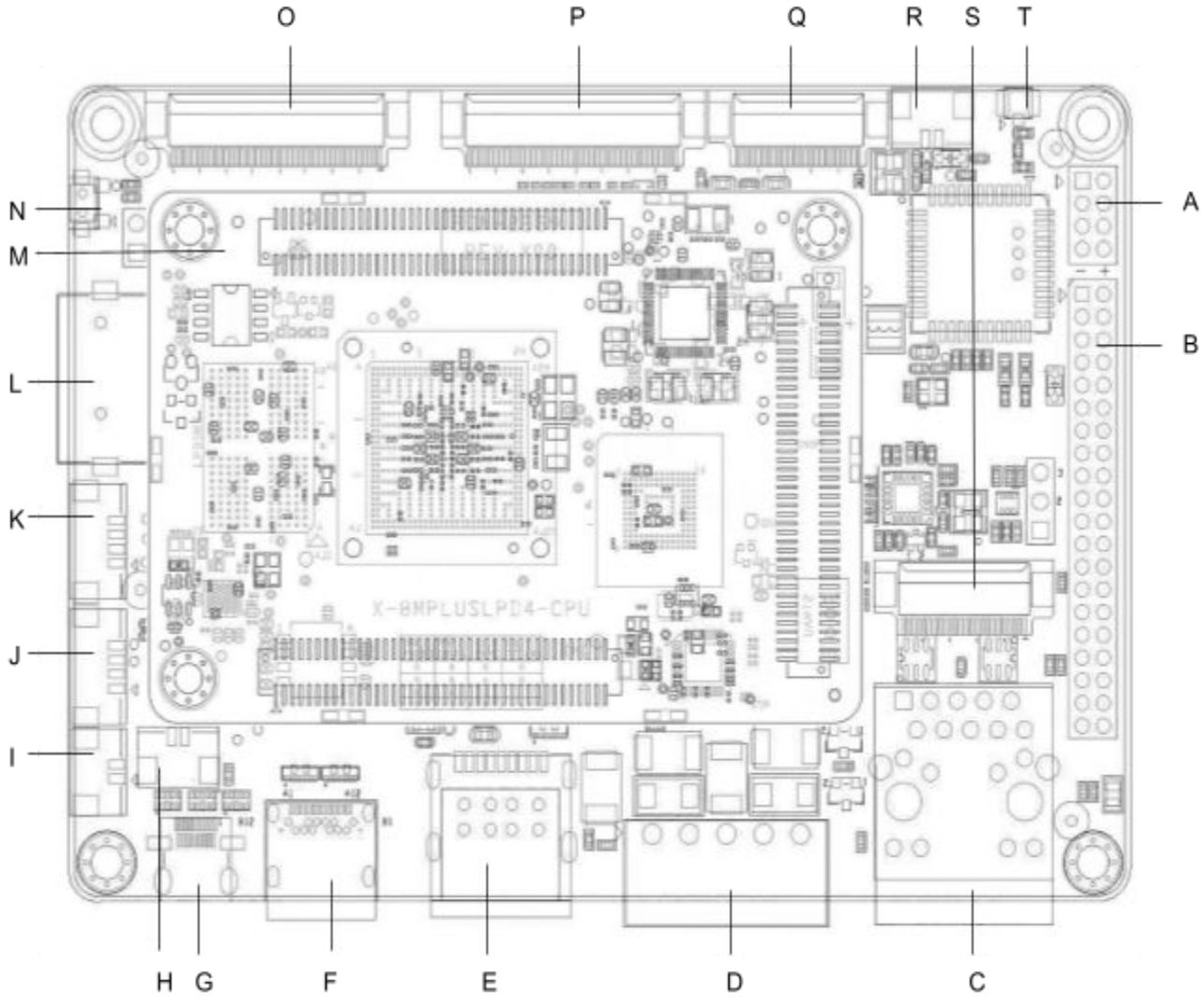

Figure1. Board Layout

Table 2. Components Show in Figure 1

Item from Figure 1	Connector	Description
A	J16	2 x USB 2.0 Host header
B	J15	5V DC in,3.3V out, PCIe signals, SAI-In, UART, Power-on, Reset, I2C, GPIOs, POE power signals

C	U13	RJ45 connector for 1000M Ethernet with POE power in support
D	J7	Modbus for RS232 or RS485 or CAN or GPIOs
E	J21A/B	USB Type A 1 x USB 3.0 Host or 2x USB 2.0 Host
F	J20	USB Type C for 1 x OTG USB 3.0 + Power Input
G	J10	Micro HDMI connector for HDMI port
H	J4	Amplified Speaker Out (R)
I	J3	Mono Speaker out or Amplified Speaker Out (L)
J	J6	L/R HP out
K	J5	2x digital MEMS microphone in
L	J9	micro SD socket
M	J17,18,19	SOM with CPU, eMMC, RAM, Codec and Ethernet PHY
N	S1	Bootload Button for eMMC flash
O	J13	FPC connector for LVDS, I2C and GPIOs
P	J12	FPC connector for MIPI DSI, MIPI CSI1, I2C GPIOs
Q	J11	FPC connector MIPI CSI2
R	J1	RTC Battery input
S	J14	Second RGMII or SAI1
T	J8	2.4/5G antenna for Wifi/BTE
LED	D3	Green LED on for system power OK
LED	D5	Red LED light for power over voltage

2.3 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.

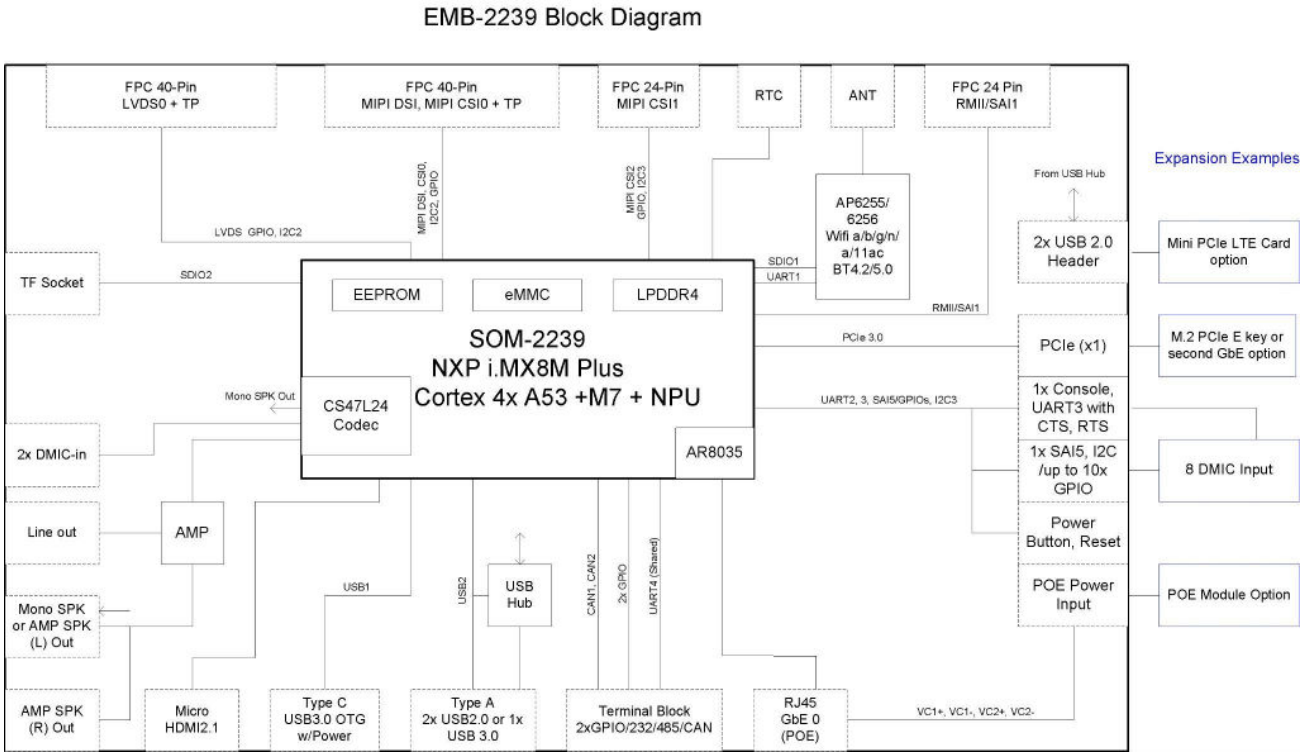

Figure 2. Block Diagram

2.4 Dimensions

Figure 3 is board layout dimensions (unit: mm).

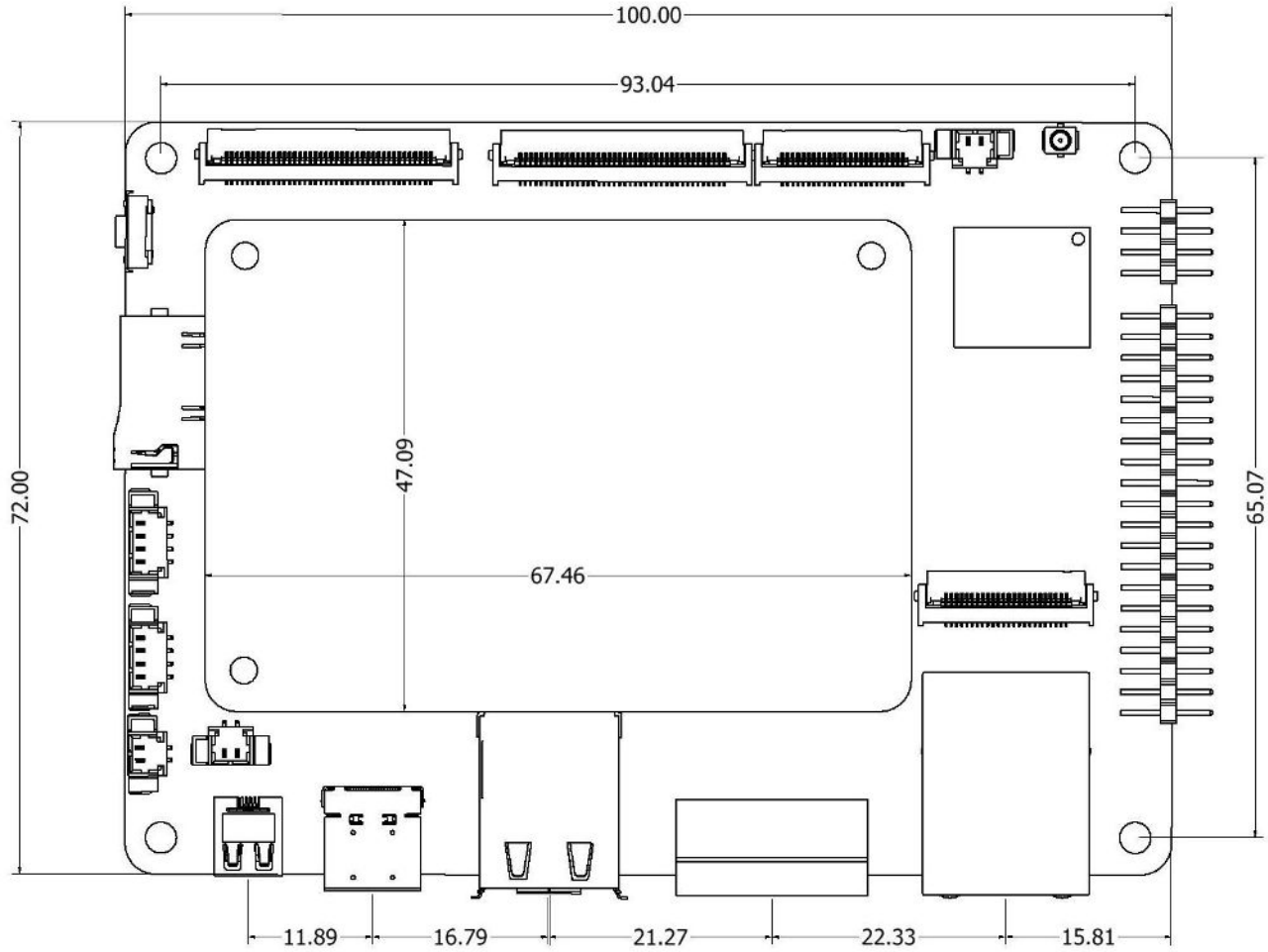

Figure 3. Dimensions

3. Technical Reference

3.1 Connectors and Headers

Table 4. J6 USB Header (Figure. 1. A)

Pin	Signal Name
1	GND
3	USB_HOST3_DP
5	USB_HOST3_DN
7	USB 5V
2	GND
4	USB_HOST4_DP
6	USB_HOST4_DN
8	USB 5V

Table 5. J15 40-pin Expansion Header (Figure. 1. B)

Pin	Signal Name	Pin	Signal Name
1	GND	21	GPIO/SAI5MCLK (3.3V)
2	+5V IN	22	GPIO/REF_CLK_32K (3.3V)
3	PCIeCLK_N (2.5V)	23	UART3_CTS/GPIO (3.3V)
4	+5V IN	24	GPIO/I2C3_SCL (3.3V)
5	PCIeCLK_P (2.5V)	25	GPIO/SAI5_RXD0 (3.3V)
6	+5V_IN	26	GPIO/I2C3_SDA (3.3V)
7	GND	27	GPIO/SAI5_RXD1 (3.3V)
8	+3.3V OUT	28	UART3_RTS/GPIO (3.3V)
9	PCIeTX_N (2.5V)	29	GPIO/SAI5_RXD2 (3.3V)
10	PWR_BTN	30	GPIO/SAI5_RXD3 (3.3V)
11	PCIeTX_P (2.5V)	31	GND
12	BootLoad_BTN	32	GND
13	GND	33	VC1+ (POE Power In)
14	GND	34	VC2+ (POE Power In)
15	PCIeRX_N (2.5V)	35	VC1- (POE Power In)
16	GPIO/UART2_TX (Console)	36	VC2- (POE Power In)
17	PCIeRX_P (2.5V)	37	GND
18	GPIO/UART2_RX (Console)	38	GND
19	GND	39	UART3_TXD
20	GND	40	UART3_RXD

Table 6. J7 Modbus Port (Figure. 1. D)

Zero ohm resistor populated option	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5
1: R20, R21, R53, R56 (default)	GPIO_A	GPIO_B	GND	RS232_TX	RS232_RX
2: R28, R32, R53, R56	GPIO_A	GPIO_B	GND	RS485_A	RS485_B

3: R36, R49, R53, R56	GPIO_A	GPIO_B	GND	CAN_H	CAN_L
4: R29, R34, R20, R21	RS485_A	RS485_B	GND	RS232_TX	RS232_RX
5: R37, R50, R20, R21	CAN_H	CAN_L	GND	RS232_TX	RS232_RX
6: R37, R50, R28, R32	CAN_H	CAN_L	GND	RS485_A	RS485_B

Table 7. J21A USB 2.0 Type A Header (Figure. 1. E, default)

Pin	Signal Name
1	USB_HOST_VBUS
3	USB_HOST1_DN
5	USB_HOST1_DP
7	GND
2	USB_HOST_VBUS
4	USB_HOST2_DN
6	USB_HOST2_DP
8	GND

Table 8. J21B USB 3.0 Type A Header (Figure. 1. E, option)

Pin	Signal Name
1	USB_HOST_VBUS
2	USB2_HS2_DN
3	USB2_HS2_DP
4	GND
5	USB2_RXN
6	USB2_RXP
7	GND
8	USB2_TXN
9	USB2_TXP

Table 9. J20 OTG Type C 3.1 Port (Figure. 1. F)

Pin	Signal Name	Pin	Signal Name
A1	GND	B1	GND
A2	SSTXP1	B2	SSTXP2
A3	SSTXN1	B3	SSTXN2
A4	OTG_PWR	B4	OTG_PWR
A5	CC1	B5	CC2
A6	USB_DP	B6	LVDS1_TX2_P
A7	USB_DN	B7	LVDS1_TX2_N
A8	SBU1	B8	SBU2
A9	OTG_PWR	B9	OTG_PWR
A10	SSRXN2	B10	SSRXN1

A11	SSRXP2	B11	SSRXP1
A12	GND	B12	GND

Table 10. J10 Micro HDMI Port (Figure. 1. G)

Pin	Signal Name
1	HPD_OUT
2	N/C
3	HDMI_D2P
4	GND
5	HDMI_D2N
6	HDMI_D1P
7	GND
8	HDMI_D1N
9	HDMI_D0P
10	GND
11	HDMI_D0N
12	HDMI_CLKP
13	GND
14	HDMI_CLKN
15	HDMI_CEC_OUT
16	GND
17	HDMI_DDC_CLK_OUT
18	HDMI_DDC_DAT_OUT
19	HDMI_5V_OUT

Table 11. J4 Amplified Speaker Out (R) Header (Figure. 1. H)

Pin	Signal Name	Pin	Signal Name
1	SPKOUTP	2	SPKOUTN

Table 12. J3 Mono Speaker Out Header (Figure. 1. I)

Pin	Signal Name	Pin	Signal Name
1	SPKOUTP	2	SPKOUTN

Table 13. J6 Headphone Out (Figure. 1. J)

Pin	Signal Name (Default)	
1	NC	
2	GND	
3	HP_out (R)	
4	HP_out (L)	

Table 14. J5 DMIC In (Figure. 1. K)

Pin	Signal Name
1	MICBIAS1
2	GND
3	DMICCLK
4	DMICDAT

Table 15. J13 LVDS and TP Header (Figure. 1. O)

Pin	Signal Name	Pin	Signal Name
1	+5V_LCD	21	LVDS1_TX0_N
2	5V_LCD	22	GND
3	GPIO_LVDS_1/BL_PWM	23	LVDS1_TX1_P
4	GND	24	LVDS1_TX1_N
5	LVDS0_TX0_P	25	GND
6	LVDS0_TX0_N	26	LVDS1_TX2_P
7	GND	27	LVDS1_TX2_N
8	LVDS0_TX1_P	28	GND
9	LVDS0_TX1_N	29	LVDS1_CLK_P
10	GND	30	LVDS1_CLK_N
11	LVDS0_TX2_P	31	GND
12	LVDS0_TX2_N	32	LVDS1_TX3_P
13	GND	33	LVDS1_TX3_N
14	LVDS0_CLK_P	34	GND
15	LVDS0_CLK_N	35	I2C2_33_SCL
16	GND	36	I2C2_33_SDA
17	LVDS0_TX3_P	37	GPIO_LVDS_2/DSI_EN
18	LVDS0_TX3_N	38	GPIO_LVDS_3/TP_nINT
19	GND	39	GPIO_LVDS_4/TP_RST
20	LVDS1_TX0_P	40	3.3V_VDDIO

Table 16. J12 MIPI CSI1 DSI Header (Figure. 1. P)

Pin	Signal Name	Pin	Signal Name
1	+5V_LCD	21	I2C3_SCL/GPIO4_MIPI
2	5V_LCD	22	I2C3_SDA/GPIO5_MIPI
3	GPIO1_MIPI/OV2_CLK	23	GPIO6_MIPI/TP_RST
4	GPIO2_MIPI/TP_nINT	24	GPIO7_MIPI/DSI_EN
5	GPIO3_MIPI/CSI_PWR_EN	25	GPIO8_MIPI/BL_PWM
6	CSI1_CLK_P	26	GND
7	CSI1_CLK_N	27	DSI_CLK_P
8	GND	28	DSI_CLK_N
9	CSI1_D0P	29	GND
10	CSI1_D0N	30	DSI_D0P
11	GND	31	DSI_D0N

12	CSI1_D1P	32	GND
13	CSI1_D1N	33	DSI_D1P
14	GND	34	DSI_D1N
15	CSI1_D2P	35	GND
16	CSI1_D2N	36	DSI_D2P
17	GND	37	DSI_D2N
18	CSI1_D3P	38	DSI_D3P
19	CSI1_D3N	39	DSI_D3N
20	GND	40	3.3V_VDDIO

Table 17. J10 MIPI CSI2 Header (Figure. 1. G)

Pin	Signal Name
1	AVDD_2.8V
2	CSI2_D0P
3	CSI2_D0N
4	GND
5	CSI2_D1P
6	CSI2_D1N
7	GND
8	CSI2_D2P
9	CSI2_D2N
10	GND
11	CSI2_D3P
12	CSI2_D3N
13	GND
14	GPIO1/OV1_CLK
15	GPIO2/CSI2_RST
16	I2C2_33_SCL
17	I2C2_33_SDA
18	GND
19	GPIO3/CSI_PWR_EN
20	AVDD_2.8V
21	DVDD_1.5V
22	VDD_1.8V
23	CSI2_CLK_P
24	CSI2_CLK_N

Table 18. J1 RTC Battery Header (Figure. 1. R)

Pin	Signal Name	Pin	Signal Name
1	RTC Battery +	2	RTC Battery -

Table 19. J14 Second RGMII / SAI1 Header (Figure. 1. S)

Pin	Signal Name
1	ETH_RX_CTL/SAI1_TXFS
2	ETH_RXC/SAI1_TXC

3	GND
4	ETH_TXD0/SAI1_TXD0
5	ETH_TXD1/SAI1_TXD1
6	ETH_TXD2/SAI1_TXD2
7	ETH_TXD3/SAI1_TXD3
8	ETH_TX_CTL/SAI1_TXD4
9	ETH_TXC/SAI1_TXD5
10	SAI1_TXD6
11	SAI1_TXD7
12	GND
13	SAI1_RXFS
14	SAI1_RXC
15	GND
16	ETH_nRST/SAI1_RXD0
17	ETH_nINT/SAI1_RXD1
18	ETH_MDC/SAI1_RXD2
19	ETH_MDIO/SAI1_RXD3
20	ETH_RXD0/SAI1_RXD4
21	ETH_RXD1/SAI1_RXD5
22	ETH_RXD2/SAI1_RXD6
23	ETH_RXD3/SAI1_RXD7
24	N/C

Table 20. Test Pads

Pin	Signal Name	Pin	Signal Name
TP1	DC5V	TP22	CLK_REQ_WIFI
TP2	VCC_RTC	TP23	GPIO_WIFI (SAI5_RXFS)
TP3	5V_AUDIO	TP24	LPO_WIFI (SLOW_CLK)
TP4-7	Amplified Speaker Out	TP25	MIPI DC5V_EXT
TP8-9	RS-232_TXD, RXD (UART4)	TP26	LVDS DC5V_EXT
TP10-12	DMIC	TP28, 38	SOM DC5V Input
TP13	RS-485_A	TP26	BOOTLOARD_KEY
TP14-15	HeadPhone Out	TP29	DC5V
TP16	RS-485_B	TP30	USB1_ID
TP17-18	CAN_H, CAN_L	TP31-36	USB_HOST1, 2
TP19	MODBUS GPIO (SPDIF_TX)	TP37	SOM SYS_nRST
TP20	MODBUS GPIO (SPDIF_RX)	TP39	BOOTLOAD_KEY
TP21	3.3V_WIFI		

3.2 Signal and Power Considerations

1. When providing power from the POE, it is not required to connect the 5V DC power input from the 40-pin header on the mainboard at the same time.
2. The VCC_5V output current from the headers output has a limit of 1A
3. The USB_5V output current from the USB headers has a limit of 1A

4. When providing power via header, make sure to provide enough current (2A or more) to the mainboard
5. Mono speaker amplifier output: 2W/CH Into 4ohm 1.4W /CH Into 8ohm.

3.3 Boot Options

The board can be selected to boot up from the on-board eMMC or micro-SD card. See Table 21.

Table 21. SW1 4bit Switch (on SOM-2239)

Bit 1 (1,8)	Bit 2 (2, 7)	Bit 3 (3, 6)	Bit 3 (4, 5)	Description
OFF	OFF	OFF	OFF	Boot from Internal Fuses
OFF	OFF	OFF	ON	Boot from USB Serial Download
OFF	OFF	ON	OFF	Boot from eMMC (default)
OFF	OFF	ON	ON	Boot from SD (SD2)

3.4 GPIO Configuration Table

Table 22. J15 40-pin Expansion Header (Figure. 1. B/Table 5)

Pad	Pin	MUX MODE						
		ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0
SAI5_RXC	21		GPIO3_IO20					SAI5_RXC
ECSPI1_MISO	23		GPIO5_IO08				UART3_CTS	ECSPI1_MISO
SAI5_RXD0	25		GPIO3_IO21					SAI5_RXD0
SAI5_RXD1	27		GPIO3_IO22					SAI5_RXD0
SAI5_RXD2	29		GPIO3_IO23					SAI5_RXD2
UART2_TXD	16		GPIO5_IO25					UART2_TXD
UART2_RXD	18		GPIO5_IO24					UART2_RXD
GPIO1_IO00	22		ANAMIX_REF _CLK_32K					GPIO1_IO00
I2C2_SCL	24		GPIO5_IO18				PWM4_OUT	I2C2_SCL
I2C3_SDA	26		GPIO5_IO19				PWM3_OUT	I2C3_SDA
ECSPI1_SS0	28		GPIO5_IO09				UART3_RTS	ECSPI1_SS0
SAI5_RXD3	30		GPIO3_IO24					SAI5_RXD3
ECSPI1_MOSI	39		GPIO5_IO07				UART3_TX	ECSPI1_MOSI
ECSPI1_SS0	40		GPIO5_IO09				UART3_RTS	ECSPI1_SS0

Table 23. J7 Modbus Port (Figure. 1. D/Table 6)

Pad	Pin	MUX MODE						
		ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0
UART4_TXD	4	RS-232 RX, TX						UART4_TXD
UART4_RXD	5							UART4_RXD
SPDIF_TX	1		GPIO5_IO03					

SPDIF_RX	2		GPIO5_IO04					
UART3_RXD	1,4	RS-485 A, B						UART3_RXD
UART3_TXD	2,5							UART3_TXD
ECSPI1_MISO	CTS						UART3_CTS	
SAI2_TXD0	1,4	CAN A, B			FLEXCAN2_TX			
SAI2_MCLK	2,5				FLEXCAN2_RX			
SPDIF_EXT_CLK	STB		GPIO5_IO05					

Table 24. J13 LVDS Header (Figure. 1. O/Table 15)

Pad	Pin	MUX MODE						
		ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0
GPIO1_IO11	3					PWM2_OUT		GPIO1_IO11
I2C2_SCL	35		GPIO5_IO16					I2C2_SCL
I2C2_SDA	36		GPIO5_IO17					I2C2_SDA
GPIO1_IO08	37						PWM1_OUT	GPIO1_IO08
GPIO1_IO13	38		PWM2_OUT					GPIO1_IO13
GPIO1_IO09	39						PWM2_OUT	GPIO1_IO09

Table 25. J12 MIPI CSI1 DSI Header (Figure. 1. P/Table 16)

Pad	Pin	MUX MODE						
		ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0
GPIO1_IO05	3							GPIO1_IO05
GPIO1_IO13	4		PWM2_OUT					GPIO1_IO13
GPIO1_IO15	5	CCM_CLKO2	PWM4_OUT					GPIO1_IO15
I2C2_SCL	21		GPIO5_IO16					I2C2_SCL
I2C2_SDA	22		GPIO5_IO17					I2C2_SDA
GPIO1_IO06	23	CCM_EXT_CLK3	GPIO5_IO12					GPIO1_IO06
GPIO1_IO09	24						PWM2_OUT	GPIO1_IO09
GPIO1_IO11	25					PWM2_OUT		GPIO1_IO11

Table 26. J11 MIPI CSI2 Header (Figure. 1. Q/Table 17)

Pad	Pin	MUX MODE						
		ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0
GPIO1_IO07	14	CCM_EXT_CLK4						GPIO1_IO07
GPIO1_IO06	15	CCM_EXT_CLK3						GPIO1_IO06
I2C2_SCL	16		GPIO5_IO16					I2C2_SCL
I2C2_SDA	17		GPIO5_IO17					I2C2_SDA
GPIO1_IO15	18	CCM_CLKO2	PWM4_OUT					GPIO1_IO15

Table 27. J14 Second RGMII / SAI1 Header (Figure. 1. S/Table 19)

Pad	Pin	MUX MODE						
		ALT6	ALT5	ALT4	ALT3	ALT2	ALT1	ALT0
SAI1_TXFS	1		GPIO4_IO10	ENET1_RGMII_RX_CTL				SAI1_TXFS
SAI1_TXC	2		GPIO4_IO11	ENET1_RGMII_RXC				SAI1_TXC
SAI1_TXD0	4		GPIO4_IO12	ENET1_RGMII_TD0				SAI1_TXD0
SAI1_TXD1	5		GPIO4_IO13	ENET1_RGMII_TD1				SAI1_TXD1
SAI1_TXD2	6		GPIO4_IO14	ENET1_RGMII_TD2				SAI1_TXD2
SAI1_TXD3	7		GPIO4_IO15	ENET1_RGMII_TD3				SAI1_TXD3
SAI1_TXD4	8		GPIO4_IO16	ENET1_RGMII_TX_CTL				SAI1_TXD4
SAI1_TXD5	9		GPIO4_IO17	ENET1_RGMII_TXC				SAI1_TXD5
SAI1_TXD6	10		GPIO4_IO18	ENET1_RX_ER				SAI1_TXD6
SAI1_TXD7	11		GPIO4_IO19	ENET1_TX_ER				SAI1_TXD7
SAI1_RXFS	13		GPIO4_IO00	ENET1_1588_EVENT0_IN				SAI1_RXFS
SAI1_RXC	14		GPIO4_IO01	ENET1_1588_EVENT0_OUT				SAI1_RXC
SAI1_RXD0	16		GPIO4_IO02	ENET1_1588_EVENT1_IN				SAI1_RXD0
SAI1_RXD1	17		GPIO4_IO03	ENET1_1588_EVENT1_OUT				SAI1_RXD1
SAI1_RXD2	18		GPIO4_IO04	ENET1_MDC				SAI1_RXD2
SAI1_RXD3	19		GPIO4_IO05	ENET1_MDIO				SAI1_RXD3
SAI1_RXD4	20		GPIO4_IO06	ENET1_RGMII_RD0				SAI1_RXD4
SAI1_RXD5	21		GPIO4_IO07	ENET1_RGMII_RD1				SAI1_RXD5
SAI1_RXD6	22		GPIO4_IO08	ENET1_RGMII_RD2				SAI1_RXD6
SAI1_RXD7	23		GPIO4_IO09	ENET1_RGMII_RD3				SAI1_RXD7

4. Operating System

4.1 Host Operating System

a. Host OS:Ubuntu 16.04 64-bit or newer
b. Host Build System: Yocto Embedded Linux

4.2 Target Operating System

a. Board u-boot version: based on NXP v2021.04
b. Board kernel version: based on NXP LF5.10.52_2.1.0
c. UI framework: Qt version 5.15.2, Wayland
d. Embedded Linux Distribution: Hardknott 3.3
e. Amazon AVS Device SDK V.1.20.0
f. Support Sensory TrulyHandsfree Wake Word Engine 6.17.0
g. BSP: https://wiki.estonetech.com/index.php?title=EMB-2239

4.3 U-boot Features

a. Support 7", 10" LVDS and MIPI LCD panel option (models: Rocktech RK070CU01, RK070BI43E, RK101II01D, G101EVN01.x, G101UAN02.0)
b. Support MFG tool image update via OTG with push button
c. Support HDMI display

4.4 Kernel Features

a. Based on NXP LF5.10.52_2.1.0
b. Support HDMI and LCD display
c. Support analog speaker, digital audio interfaces
d. WiFi support (AP6255/56)
e. BT support on data, audio in and out (AP6255/56)

4.5 Other OS Support

a. Android Android 10
b. Linux Debian 9, 10

Refer to https://wiki.estonetech.com/index.php?title=EMB-2239 for instructions on building the file systems.